Design and Characterization of High Performance 60 GHz Pseudomorphic MODFET LNAs in CPW-Technology Based on Accurate S-Parameter and Noise Models

M. Schlechtweg, W. Reinert, P.J. Tasker, R. Bosch, J. Braunstein, A. Hülsmann, K. Köhler

Fraunhofer-Institut für Angewandte Festkörperphysik
Tullastrasse 72, 7800 Freiburg, Germany
Phone: 0049/761-5159534, Fax: 0049/761-5159400

Abstract

We have fabricated low noise V-band 2-stage amplifiers using PM-MODFETs which have a performance of 10.5 dB gain and 5.2 dB noise figure at 58.5 GHz in very close agreement with results predicted in advance. The CAE models for the transistors and the passive CPW-components were extracted from on-wafer S-parameter measurements up to 60 GHz and noise parameter measurements up to 18 GHz. For noise modeling of the MODFETs up to millimeter wave frequencies, we have pursued a novel approach which is based on the temperature noise model reported by Pospiezalski [1]. A very good agreement between simulated and measured MMIC gain and noise performance is achieved up to V-band using these models.

Introduction

Monolithically integrated millimeter wave circuits in the frequency region above 40 GHz are reaching production state for various applications including inter-satellite communications, environmental survey systems, and various radar applications, e.g. collision avoidance radar. A key system component of front end receivers is the low noise amplifier, which has been the focus of our activities. For volume production with high yield and predictable circuit performance, however, a reproducible IC-technology is required in conjunction with accurate CAE models for the active and passive circuit components.

Transistor Modeling

Our circuit design approach comprises accurate on-wafer S-parameter characterization and modeling of all circuit components up to 60 GHz. The active devices are

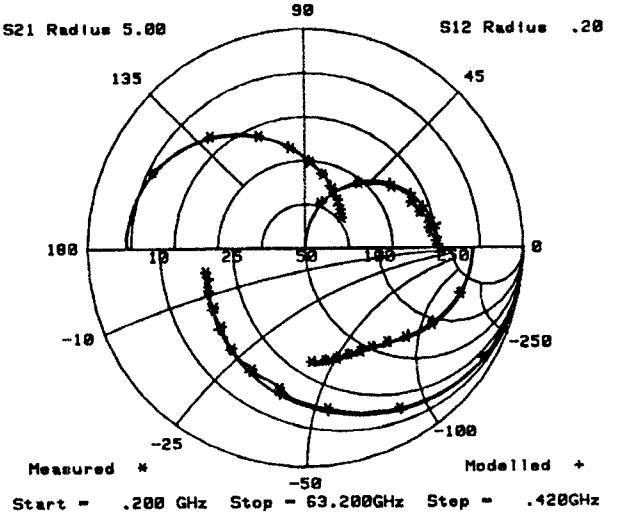

Fig. 1 Measured and calculated S-parameters of a 0.3 μm x 100 μm PM-MODFET in the frequency range from 0.2 GHz to 63.2 GHz.

PM-MODFETs (25% In mole fraction) on GaAs substrate which have demonstrated at smaller gate lengths transit frequencies of 120 GHz [2,3]. At millimeter wave frequencies, physically relevant transistor models are needed to predict the performance of the MMIC correctly. An important issue is the modeling of the parasitic capacitances of the FETs. We have studied in detail the FET parasitics as a function of transistor geometry and layout using dummy FET test structures on isolated semiconductor material. The parasitic pad-capacitances of the FET have been extracted by two different methods with an agreement of better than 1 fF [4]. Using this database, a very good agreement between measured and modeled S-parameters of the active transistor (gate geometry 0.3 μm x 100 μm) is achieved up to 63 GHz as can be seen in Fig. 1. This shows clearly, that a transistor of this gate width can be modeled very accurately by a

92CH3162-5/92/0000-0029$01.00 © 1992 IEEE

lumped element circuit model and there is no need to use a much more complicated model with distributed elements.

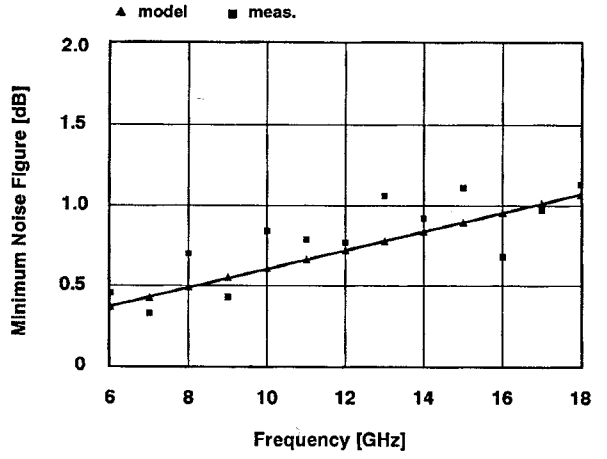

Fig. 2 Minimum noise figure of a 0.3 μm x 100 μm PM-MODFET, measured and calculated with the temperature model.

To predict the noise performance of the transistors at millimeter wave frequencies, we have employed a transistor noise temperature model which is based on the method proposed in [1]. With the temperature noise model, the noise parameters of the FET can be determined from the circuit model assigning an equivalent noise temperature to each resistive model element. Our calculations were done by assigning ambient temperature to all resistors with the exception of the channel resistance R_{ds}, wich has a higher noise temperature T_{out}.

In the first step, a physically relevant equivalent circuit model of the transistor is derived. Then the noise parameters of the transistor are measured on-wafer up to 18 GHz. The model output temperature T_{out}, which is the only remaining parameter needed for the noise model, is extracted by fitting the noise parameters calculated from the equivalent circuit to the measured data. The FET temperature noise model was implemented in the commercial Eesof software. A comparison between the calculated and measured minimum noise figure of a 0.3 μm x 100 μm PM-MODFET is given in Fig. 2.

Modeling of CPW-Structures

We have chosen coplanar waveguide technology because of the advantages regarding technological issues (no substrate thinning or via hole technology required) and circuit performance (grounding of components without additional parasitics, lower transmission line dispersion). All circuit relevant CPW-structures, e.g. homogeneous transmission lines, T-junctions, in-line series overlay capacitors, bias circuitry, were separately characterized up to 60 GHz. The related model parameters were extracted from this data. For this purpose, a mask set with passive test structures was developed.

We have shown recently the strong influence of the finite metallization thickness on transmission line parameters [5]. For millimeter wave applications, frequency dispersion phenomena with respect to the effective dielectric constant and the characteristic impedance have to be taken into account. Coplanar lines exhibit a decreasing effective dielectrict constant $\varepsilon_{r,eff}$ with increasing frequency, in contrast to microstrip structures. The dispersive propagation characteristics of CPWs, however, are substantially lower compared to microstrip transmission lines [6].

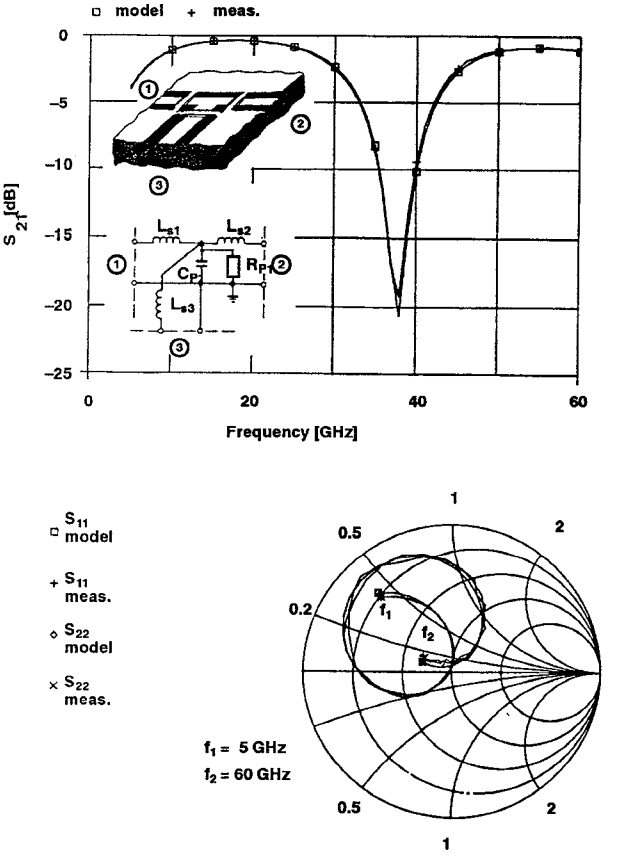

Fig. 3 Measured and modeled two port S-parameters of a CPW T-junction. Port 3 is terminated by a short-circuited transmission line.

As an example for CPW-discontinuities, the modeled and measured S-parameters of a coplanar T-junction with a shorted stub connected at the third port (characteristic impedance of all lines 50 Ω) are shown in Fig. 3, showing very good agreement. To model the discontinuity, a simple 5-element equivalent circuit model was used as given in Fig. 3.

Circuit Design

For the verification of basic circuit design concepts, simple single stage MMIC amplifier circuits have been designed in the 40 to 60 GHz region. We have reported results on these single stage MODFET amplifiers recently, which delivered a gain of 9.5 dB, 7.0 dB and 5.0 dB at 40 GHz, 50 GHz and 60 GHz, respectively [4].

Based on these results, fully integrated 2-stage amplifier MMICs were designed. The MMICs include all matching networks and bias subcircuits. The gate geometry of the transistors in the amplifiers is 0.3 μm x 80 μm. The interstage matching network was designed to give a direct impedance transformation between the stages instead of transforming to an impedance of 50 Ω. An important design focus was the stability of the circuits, because previous investigations had shown that the amplifiers could tend to oscillate at frequencies between 20 GHz and 30 GHz. Therefore, stability criteria were included in the optimimization routine using the CAE tool. As a result of this approach, the realized amplifier circuits were unconditionally stable with a stability factor k>1.5 over the entire frequency region. The circuit topology of the LNA is depicted in Fig. 4.

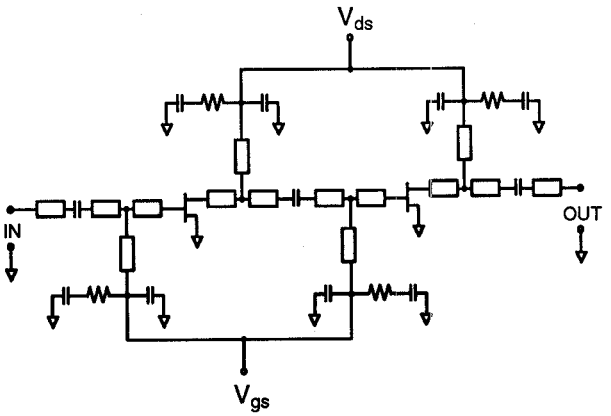

Fig. 4 Circuit Topology of the 2-stage LNA.

MMIC Characterization

The MMICs were fabricated including airbridges, MIM-capacitors and NiCr-resistors. Our MMIC process uses a dry gate-recess which yields a high uniformity of the FET parameters across the wafer. Pattern definition is performed using a 'mix and match' e-beam/optical lithography.

The LNAs were characterized with an on-wafer S-parameter measurement system which is based on a HP 8510C network analyzer system extended by a mm-wave test set to 63 GHz. The network analyzer was calibrated using the LRM calibration method.

To make accurate noise figure measurements possible at V-band frequencies, we have developed an on-wafer noise measurement system in the 55 to 60 GHz range. In order to achieve high measurement accuracy, the ENR of the noise diode at the waveguide reference plane was determined by a hot/cold measurement of a waveguide load at 300 K and 77 K, respectively. Furthermore, the S-parameters of the waveguide/coaxial-transition and wafer probe head were determined. Using this data, the ENR at the coplanar reference plane was calculated. An HP 8970B noise figure meter was used in the measurement set up.

A micrograph of the LNA chip is shown in Fig. 5. The chip size of the amplifier is 2.2 x 1.8 mm^2. The bias pads are configured compatible to the Cascade RF probe heads to facilitate automatic measurements. The measured and calculated gain and noise figure of the MMIC is shown in Fig. 6. No additional tuning elements were added to achieve the reported performance.

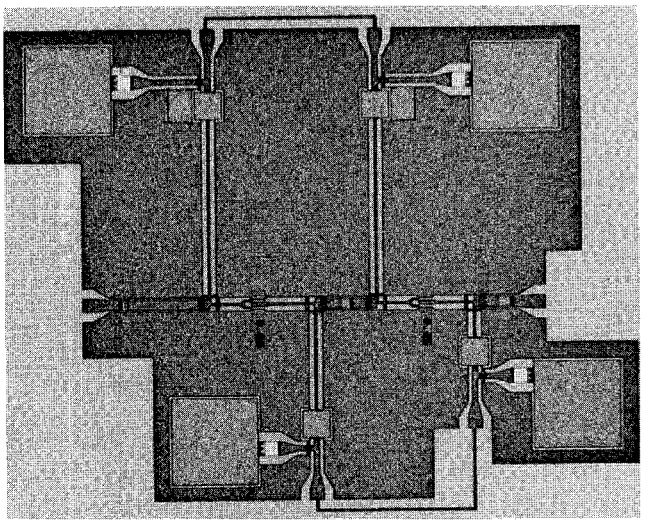

Fig. 5 Micrograph of the 2-stage LNA Chip.

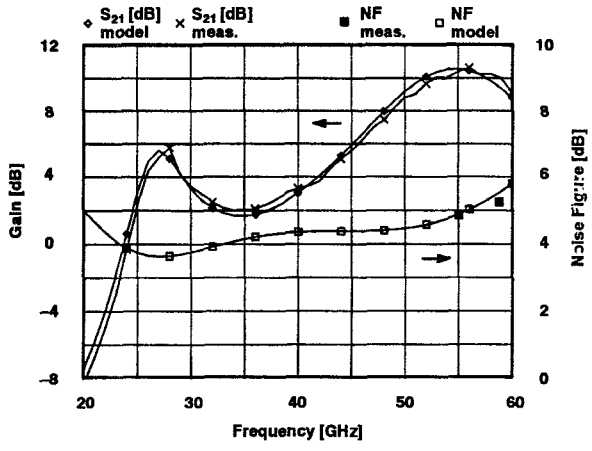

Fig. 6 Gain and noise performance of the 2-stage V-band LNA.

Conclusion

We have developed an accurate CAE database for active and passive MMIC components. The models were verified by on-wafer measurements up to 60 GHz. Based on these results, a V-band LNA was designed which has a state-of-the-art performance showing a gain of 10.5 dB and a noise figure of 5.2 dB at 58.5 GHz, respectively. This compares favourably to previous results of a Microstrip LNA with PM-MODFETs of similar gate length published in [7]. Due to the moderate gate length of 0.3 µm and the reproducible technology process, the circuit yield was better than 80%.

Acknowledgement

The authors would like to thank T. Jakobus and his group for MMIC-processing, W. Haydl for valuable discussions and H. S. Rupprecht for continous encouragement of the work.

Literature

[1] M. W. Pospiezalski, "Modeling of Noise Parameters of MESFETs and MODFETs and their Frequency and Temperature Dependence", IEEE Trans. MTT, Vol. MTT-37, pp. 1340-1350, 1989.

[2] A. Hülsmann et al., "Mushroom shaped gates defined by e-beam lithography down to 80 nm gate lengths and fabrication of pseudomorphic HEMTs with a dry etched gate recess", Proceedings of the 1991 SPIE Symposium, Paper 1465-26.

[3] J. Braunstein et al., "Investigation of Transport Phenomena in Pseudomorphic HEMTs", GaAs and Related Compounds Conference, Seattle, Sept. 1991.

[4] M. Schlechtweg et al., "Monolithic Millimeter-Wave CPW Amplifiers with 0.25µm Gate Pseudomorphic MODFETs in the 40 to 60 GHz Frequency Range", Proc. 15th European Workshop on Compound Semiconductor Devices and Integrated Circuits, Grönenbach 1991.

[5] W. H. Haydl et al., "Millimeter-Wave Coplanar Transmission Lines on Gallium Arsenide, Indium Phosphide and Quartz with Finite Metalization Thickness", 1991 MTT-S Symposium Digest, p. 691.

[6] W. Heinrich, "Full Wave-Analysis of Conductor losses on MMIC Transmission Lines", IEEE Trans. MTT, Vol. 38, No. 10, pp. 1468-1472, Oct. 1990.

[7] G. M. Metze et al., "60-GHz Pseudomorphic-MODFET Low-Noise MMIC Amplifiers", IEEE Electron Device Letters, Vol. EDL-10, pp. 165-176, 1989.